Amendments to the Specification:

Please amend Paragraph [0021] as follows:

[0021] Figure 1, illustrates a partial cross-section view of an integrated circuit 100 of one embodiment of the present invention. In this embodiment, the part of the integrated circuit 100 shown includes a N-channel MOS power device 102, a N-DMOS device 104 and a NPN bipolar device 106. As Figure 1 also illustrates three conductive layers, which in this embodiment includes a first metal layer M1 108, a second metal layer M2 110 and a third metal layer M3 112. The metal layers 108, 110, and 112 can be made of conductive material such as aluminum, copper and the like. Moreover, in another embodiment, at least one of the metal layers 108, 110 and 112 is made by a sub-micron process that forms many sub-layers of alternating conductive layers. The third metal layer M3 112 can be referred to as the top metal layer 112. As illustrated, a bond pad 130 is formed on a surface of the third metal layer M3 112 by patterning a passivation layer 132. A ball bond wire114 (bond wire 114) can be coupled to the bonding pad 130 to provide an input or output to the integrated circuit 100. Although, this embodiment, only illustrates three metal layers 108, 110 and 112, other embodiments have more or less metal layers. For example, in an embodiment with more than three metal layers, additional metal layers are formed between metal layers 108 and 110. Each interconnect metal layer 108, 110 and 112 is formed by conventional methods known in the art such as depositing and patterning.